ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS
(Choice Based Credit System)

R24

VLSI SYSTEM DESIGN

For

Master of Technology (M.Tech)

(Applicable for batches admitted from 2024-2025)

SWARNANDHRA

COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

SEETHARAMAPURAM, NARSAPUR-534 280, W.G.DT., A.P.

1. INTRODUCTION

Swarnandhra College of Engineering & Technology (Subsequently referred to as SCET) will be followed the norms of Jawaharlal Nehru Technological University Kakinada and Govt. of Andhra Pradesh.

Academic Programmes of the institute are governed by rules and regulations approved by the Academic Council, which is the highest Academic body of the Institute. These rules and regulations are applicable for the students of M. Tech (Regular) Course from the Academic Year 2019-20 onwards.

2. ADMISSIONS:

2.1. Admission into first year of M. Tech Programme: Admissions in each M.Tech program in the Institution are classified into **CATEGORY - A** through convener, PGECET and **GATE. CATEGORY- B** seats are filled by the college management.

2.2. Admissions with advance standing: These may arise in the following cases:

a) When a student seeks transfer from other colleges to SCET and desirous to pursue the study at SCET in an eligible branch of study.
b) When students of SCET get transferred from one regulation to another regulation or from previous syllabus to revised syllabus.
c) When a student after long discontinuity rejoins the college to complete his/her Program of study for the award of degree.

In all such cases for admission, when needed, permissions from the statutory bodies are to be obtained and the Programme of study at SCET will be governed by the transitory regulations.

3. DURATION OF THE PROGRAMME AND MEDIUM OF INSTRUCTION:

The duration of the M. Tech. Program is two academic years consisting of four semesters. Students, who fail to fulfill all the academic requirements for the award of the degree within minimum of four academic years, will forfeit their admission in M. Tech course**.** The medium of instruction and examinations are in English.

4. PROGRAMMES OF STUDY:

The following specializations are offered at present.

i) M. Tech – Power Electronics
ii) M. Tech – CAD/CAM

iii) M. Tech – VLSI System Design

iv) M. Tech – Communication Systems

v) M. Tech – Computer Science & Engineering

vi) M. Tech – Thermal Engineering

vii) M. Tech – Structural Engineering

5. AWARD OF M. TECH DEGREE

- The candidate pursues a course of study in not less than two and not more than four academic years.
- The student shall register for all 68 credits and secure the same.

6. ATTENDANCE

The minimum instruction days in each semester are 90.

i. A student will be eligible to appear for end semester examinations, if he/she acquired a minimum of 75% of attendance in aggregate of all the courses.

ii. Condonation of shortage of attendance in aggregate up to 10% on medical grounds (Above 65% and below 75%) in any semester may be granted by the College Academic Committee.

iii. Shortage of Attendance below 65% in aggregate shall not be condoned

iv. Students with less than 65% of attendance in any semester are not eligible to take up their end examination of that particular semester and their registration for examination shall be allowed.

v. Attendance may also be condoned for those who participate in Intercollegiate/university sports, co- and extracurricular activities provided their attendance is in the minimum prescribed range for the purpose (>65%) and recommended by the concerned authority. He/ She shall pay the prescribed condonation fee.

vi. Prescribed Condonation fee shall be payable by the student to appear for the end examination.

vii. A Student will not be promoted to the next semester unless he/she satisfies the attendance requirement of the present semester as applicable. They may seek re-admission for that semester as and when offered consecutively by the Department.

7. EVALUATION

- The performance of the candidate in each semester shall be evaluated course-wise, with a maximum of 100 marks for both theory and practical, on the basis of Internal Evaluation and End Semester Examination.
- For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation.

7.1 Continuous Internal Evaluation:

Theory

(a) For theory subjects, during a semester, there shall be two mid-term examinations. Each midterm examination shall be conducted for a total duration of 120 minutes with 4 questions (without choice) each question for 10 marks.

(b) The descriptive examination is set with 4 full questions from first two and half units (50% of the syllabus), the student has to answer all questions. In the similar lines, descriptive examination shall be conducted on the rest of the syllabus.

(c) The first mid (Mid-1) marks shall be submitted to the examination section within one week after completion of first mid examination.

(d) The mid marks submitted to the examination section shall be displayed in the concerned department notice boards for the benefit of the students.

(e) If any discrepancy found in the submitted Mid-1 marks, it shall be brought to the notice of examination section within one week from the submission.

(f) Second mid examination shall be conducted on the similar lines of mid-1 and its mid (Mid-2) marks shall also be submitted to examination section within one week after completion of second mid examination and it shall be displayed in the notice boards. If any discrepancy found in the submitted mid-2 marks, it shall be brought to the notice of examination section within one week from the submission.

(g) The final marks are the sum of average of two mid-term examinations i.e. $\frac{\text{Mid1+Mid2}}{2}$

7.2 End Semester Theory Examination Evaluation:

Theory:

- End semester examination is conducted for 60 marks. Question paper consists of five questions from five units with internal choice. Duration of exam is 180 minutes.

7.3 Laboratory Evaluation:

Internal Evaluation: The internal marks for laboratory are 40 marks and the marks shall be awarded based on the day to day work: 10 marks, Record: 5 marks and the remaining 25 marks to be awarded by conducting an internal laboratory test.

External Evaluation: For external marks for laboratory are 60 and marks shall be awarded based on the performance in the end laboratory examinations. Laboratory examination must be conducted with two Examiners, one of them being the Laboratory Class Teacher and the second examiner shall be appointed by the COE from the panel of examiners submitted by the respective college. Laboratory examination must be conducted with a breakup marks of Procedure-15, Experimentation-25, Results-10, Viva-voce-10.

7.4 For MOOCs Course, the student shall register for the course (Minimum of 12 weeks) offered by SWAYAM/NPTEL/JNTUK MOOCs through online with the approval of committee comprises of Head of the Department and two senior faculty. The Head of the Department shall appoint one mentor for each of the MOOC courses offered. The student needs to earn a certificate by passing the exam. The student will be awarded the credits given in curriculum only by submission of the certificate.

7.5 A candidate shall be deemed to have secured the minimum academic requirement in a course if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the end semester Examination and Internal.

7.6 A candidate shall be given one chance to re-register for each course provided the internal marks secured by a candidate are less than 50% and has failed in the end examination after completion of the third semester. The candidate's attendance in the re- registered course(s) shall be calculated separately to decide upon his/her eligibility for writing the end examination in those courses(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled. For re-registration the candidates have to apply to the Institute by paying the requisite fees and get approval from the concern authorities before the start of the semester in which re-registration is required. In case the candidate secures less than the required attendance in any re-registered course(s), he/she shall not be permitted to write the End Examination in that course.

7.7 Laboratory external examination must be conducted with internal and external examiner. External examiner will be appointed by the COE from the approved panel of examiners.

7.8 For non-credit Audit Courses, "Satisfactory" or "Unsatisfactory" shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA/Percentage

7.9 For Mini Project with Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other senior faculty members of the department. For Mini Project with Seminar, there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

8. EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

i. A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members in the department.

ii. Registration of Dissertation/Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

iii. After satisfying (ii), a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval. The student can initiate the Project work, only after obtaining the approval from the Project Review Committee (PRC).

iv. If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Project Review Committee (PRC). However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

v. Continuous assessment of Dissertation-I and Dissertation-II during the Semester(s) will be monitored by the PRC.

vi. A candidate shall submit his status report in two stages to the PRC, at least with a gap of 3 months between them.

vii. The work on the project shall be initiated at the beginning of the 3rd Semester and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical subjects before submission of the Thesis.

viii. Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.

ix. The thesis shall be adjudicated by one examiner from the approved panel of examiners, by the COE.

x. Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination. The Board shall jointly report the candidate's work as one of the following:

A. Excellent

B. Good

C. Satisfactory

D. Unsatisfactory

If the report of the Viva-Voce is unsatisfactory, the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the Concern authorities.

9. GRADING SYSTEM:

9.1 Computation of SGPA

The following procedure is to be adopted to compute the Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

The SGPA is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.,

$$SGPA\ (Si) = \sum (Ci \times Gi) / \sum Ci$$

Where C_i is the number of credits of the i^{th} course and G_i is the grade point scored by the student in the i^{th} course.

9.2 Computation of CGPA

The CGPA is also calculated in the same manner taking into account all the courses undergone by a student over all the semester of a programme, i.e.,

$$CGPA = \sum (Ci \times Si) / \sum Ci$$

Where Si is the SGPA of the it semester and Ci is the total number of credits in that semester. The SGPA and CGPA shall be rounded off to TWO decimal points and reported in the transcripts.

9.3 Award of Grade in Each Semester:

a. Based on the performance during a given semester, a final letter grade will be awarded at the end of the semester for each subject. The letter grades and the corresponding grade points are as given in the Table.

Marks Range(Max – 100)	Level	Letter Grade	Grade Point
≥ 90	Outstanding	A+	10
≥80 to <90	Excellent	A	9
≥70 to <80	Very Good	B	8
≥60 to <70	Good	C	7
≥50 to <60	Satisfactory	D	6
<50	Fail	F	0
-	Absent	AB	0

b. Grade Sheet: A grade sheet (memorandum) will be issued to each student indicating his performance in all courses taken in that semester and also indicating the Grades.

c. Transcripts: After successful completion of the total program of study, a Transcript containing performance of all academic years will be issued as a final record. Duplicate transcripts will also be issued up to any point of study to any student on request and by paying the stipulated fee in force.

d. Candidates shall be permitted to apply for revaluation within the stipulated period with payment of prescribed fee.

10. AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M.Tech Degree he shall be placed in one of the following four classes:

Class Awarded	CGPA to be secured	
First Class with Distinction	≥ 7.75 (Without any supplementary appearance)	**From the CGPA secured from 68 Credits.**
First Class	≥ 7.75 (With any supplementary appearance) ≥ 6.75 to < 7.75	
Second Class	≥ 6.0 to < 6.75	
Pass Class	≥ 5.0 to < 6.0	

11. CONDUCT AND DISCIPLINE:

Students admitted in SCET are to be followed the conduct and discipline of the college and which will be updated from time to time.

12. MALPRACTICES:

If any malpractices held in internal assessment tests or Semester-End Examinations, Principal constitute a Malpractice Enquiry Committee to enquire the case. The principal shall take necessary action based on the recommendations of the committee as per stipulated norms.

13. WITHHOLDING OF RESULTS

If the student has not paid the dues, if any, to the university or if any case of indiscipline is pending against him, the result of the student will be withheld. His degree will be withheld in such cases.

14. GENERAL

- Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.
- The academic regulation should be read as a whole for the purpose of any interpretation.
- In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman, Academic Council is final.
- The College may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the College.

M.TECH COURSE STRUCTURE

I SEMESTER

S.NO	Subject Code	Course Title	L	P	C	IM	EM	TM
1	24VL1T01	Advanced CMOS System Design using HDL.	3	0	3	40	60	100
2	24VL1T02	VLSI Technology and Design.	3	0	3	40	60	100
3		**PROGRAM ELECTIVE-I**	3	0	3	40	60	100
	24VL1E01	Digital System Design.						
	24VL1E02	Analog CMOS IC Design.						
	24VL1E03	Optimization Techniques in VLSI Design.						
4		**PROGRAM ELECTIVE–II**	3	0	3	40	60	100
	24VL1E04	CPLD and FPGA Architectures and Applications.						
	24VL1E05	Advanced Computer Architecture.						
	24VL1E06	Hardware Software Co-Design						
5	24CC1T01	Research Methodology and IPR.	2	0	2	40	60	100
6	24VL1L01	CMOS System Design Using VHDL Laboratory	0	4	2	40	60	100
7	24VL1L02	CMOS Layout Design Laboratory	0	4	2	40	60	100
8		Audit Course - I	2	0	0	-	-	-
TOTAL			**16**	**8**	**18**	**280**	**420**	**700**

II SEMESTER

S.NO	Subject Code	Course Title	L	P	C	IM	EM	TM
1	24VL2T01	Low Power VLSI Design	3	0	3	40	60	100
2	24VL2T02	Design for Testability	3	0	3	40	60	100
3		**PROGRAM ELECTIVE-III**	3	0	3	40	60	100
	24VL2E07	VLSI and NANO Materials						
	24VL2E08	DSP Processors & Architectures						
	24VL2E09	CAD for VLSI						
4		**PROGRAM ELECTIVE–IV**	3	0	3	40	60	100
	24VL2E10	System on Chip Design						
	24VL2E11	CMOS Mixed Signal Design						
	24VL2E12	ASIC Design and Development.						
5	24VL2L01	System Verilog Programming Laboratory	0	4	2	40	60	100
6	24VL2L02	CMOS testing and verification Laboratory	0	4	2	40	60	100
7	24VL2P01	Technical Seminar	2	0	2	50	-	50
8		Audit Course - II	2	0	0	-	-	-
TOTAL			**16**	**8**	**18**	**290**	**360**	**650**

*Student has to choose any one audit course listed at the end of the course structure.

III SEMESTER

S.NO	Subject Code	Course Title	L	P	C	IM	EM	TM
1		**PROGRAM ELECTIVE-V**	3	0	3	40	60	100
	24VL3E13	CMOS Digital IC Design						
	24VL3E14	Semiconductor Memory Design and Testing						
	24VL3E15	VLSI Signal Processing						
2		**OPEN ELECTIVE**	3	0	3	40	60	100
	24CM3O01	Business Analytics						
	24CC3O02	Industrial Safety						
	24CC3O03	Operations Research						
	24MB3O04	Cost Management of Engineering Projects						
	24CC3O05	Composite Materials						
	24PE3O06	Waste to Energy						
3	24VL3P01	Project Work Part-I	0	20	10	-	-	-
TOTAL			6	20	16	80	120	200

IV SEMESTER

S No	Subject Code	Course Title	L	P	C	IM	EM	TM
1	24VL4P02	Project Work Part-II	0	32	16	80	120	200
		TOTAL	**0**	**32**	**16**	**80**	**120**	**200**

Audit course I & II

S No	Course Code	Course Title
1	24ACXM01	English for Research Paper Writing
2	24ACXM02	Disaster Management
3	24ACXM03	Sanskrit for Technical Knowledge
4	24ACXM04	Value Education
5	24ACXM05	Constitution of India
6	24ACXM06	Pedagogy Studies
7	24ACXM07	Stress Management by Yoga
8	24ACXM08	Personality Development through Life Enlightenment skills

- X indicates semester number

M Tech 1st SEMESTER	L	P	C
	3	0	3
24VL1T01 Advanced CMOS System Design using HDL			

UNIT-I:

Digital Logic Design using **VHDL**

Introduction, designing with VHDL, design entry methods, logic synthesis , entities , architecture , packages and configurations, types of models: dataflow , behavioral , structural, signals vs. variables, generics, data types, concurrent vs. sequential statements , loops and program controls.

Digital Logic Design using Verilog HDL

Introduction, Verilog Data types and Operators, Binary data manipulation, Combinational and Sequential logic design, Structural Models of Combinational Logic, Logic Simulation, Design Verification and Test Methodology, Propagation Delay, Truth Table models using Verilog.

UNIT-II:

Combinational Logic Circuit Design using VHDL

Combinational circuits building blocks: Multiplexers, Decoders , Encoders , Code converters, Arithmetic comparison circuits , VHDL for combinational circuits , Adders-Half Adder, Full Adder, Ripple-Carry Adder, Carry Look-Ahead Adder, Subtraction, Multiplication.

Sequential Logic Circuit Design using VHDL

Flip-flops, registers & counters, synchronous sequential circuits: Basic design steps, Mealy State model, Design of FSM using CAD tools, Serial Adder Example, State Minimization, Design of Counter using sequential Circuit approach.

UNIT-III: Digital Logic Circuit Design Examples using Verilog HDL

Behavioral modeling , Data types, Boolean-Equation-Based behavioral models of combinational logics , Propagation delay and continuous assignments , latches and level-sensitive circuits in Verilog, Cyclic behavioral models of flip-flops and latches and Edge detection, comparison of styles for behavioral model; Behavioral model, Multiplexers, Encoders and Decoders, Counters, Shift Registers, Register files, Dataflow models of a linear feedback shift register, Machines with multi cycle operations, ASM and ASMD charts for behavioral modeling, Design examples, Keypad scanner and encoder.

UNIT-IV: Synthesis of Digital Logic Circuit Design

Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic with latches and flip-flops, Synthesis of Explicit and Implicit State Machines, Registers and counters.

UNIT-V: Testing of Digital Logic Circuits and CAD Tools

Testing of logic circuits, fault model, complexity of a test set, path-sensitization, circuits with tree structure, random tests, testing of sequential circuits, built in self-test, printed circuit boards, computer aided design tools, synthesis, physical design.

TEXT BOOKS:

1. Stephen Brown &ZvonkoVranesic"Fundamentals of Digital logic design with VHDL", Tata McGraw Hill, 2nd edition.
2. Michael D. Ciletti, "Advanced digital design with the Verilog HDL", Eastern economy edition, PHI.

REFERENCE BOOKS:

1. Stephen Brown & ZvonkoVranesic ”Fundamentals of Digital logic with Verilog design”, Tata McGraw Hill,2nd edition.
2. Bhaskar,”VHDL Primer”,3rd Edition, PHI Publications.
3. Ian Grout, “Digital systems design with FPGAs and CPLDs”, Elsevier Publications.

M Tech 1st SEMESTER	L	P	C
	3	0	3
24VL1T02 :: VLSI Technology and Design			

UNIT-I:

VLSI Technology: Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.

VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques,
state machine logic design techniques and design issues.

UNIT-II:

CMOS VLSI Design: MOS Technology and fabrication process of pMOS, nMOS, CMOS and Bi CMOS technologies, comparison of different processes.

Building Blocks of a VLSI circuit: Computer architecture, memory architectures, communication interfaces, mixed signal interfaces.

VLSI Design Issues: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

UNIT-III:

Basic electrical properties of MOS and Bi CMOS circuits, MOS and Bi CMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitative and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT-IV:

Subsystem Design and Layout: Some architectural issues switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.

Subsystem Design Processes: Some general considerations and an illustration of design processes, design of an ALU subsystem.

UNIT-V:

Floor Planning: Introduction, Floor planning methods, off-chip connections.

Architecture Design: Introduction, Register-Transfer design, high-level synthesis, architectures for low power, architecture testing.

Chip Design: Introduction and design methodologies.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, SholehEshraghian, 2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.
3. VLSI Design-Dr.K.V.K.K.Prasad, KattulaShyamala, Kogent Learning Solutions Inc., 2012.

REFERENCE BOOKS:

1. VLSI Design Technologies for Analog and Digital Circuits, Randall L.Geiger, Phillip E.Allen, Noel R.Strader, TMH Publications, 2010.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming-BO Lin, CRC Press,2011.
3. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2ndEdition, Addison Wesley.

M Tech 1st SEMESTER	L	P	C
	3	0	3
24VL1E01 DIGITAL SYSTEM DESIGN (ELECTIVE-I)			

UNIT-I: Minimization Procedures and CAMP Algorithm

Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP- I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II: PLA Design, PLA Minimization and Folding Algorithms

Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples

UNIT -III: Design of Large Scale Digital Systems

Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV: Fault Diagnosis in Combinational Circuits

Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V: Fault Diagnosis in Sequential Circuits

Fault detection and location in sequential circuits, circuit test approach, initial state identification, Hamming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS:

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi , 2 nd Edition, 2001, TMH
3. Digital system Design using PLDd-Lala

REFERENCE BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

M Tech 1st SEMESTER	L	P	C
	3	0	3
24VL1E02 :: Analog CMOS IC Design (ELECTIVE-I)			

UNIT –I

MOS Devices and Modeling The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT –II

Analog CMOS Sub-Circuits MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT –III

CMOS Amplifiers Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT –IV

CMOS Operational Amplifiers Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT –V

Comparators Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G.Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin,Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

M Tech 1st SEMESTER	L	P	C
	3	0	3
24VL1E03 :: Optimization Techniques in VLSI Design (ELECTIVE-I)			

UNIT-I: STATISTICAL MODELING

Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT-II: STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, Highlevel statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT-III: CONVEX OPTIMIZATION

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Polynomial fitting.

UNIT-IV: GENETIC ALGORITHM

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA-Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

UNIT-V: GA ROUTING PROCEDURES AND POWER ESTIMATION

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

TEXT BOOKS / REFERENCE BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power - AshishSrivastava, Dennis Sylvester, DavidBlaauw, Springer, 2005.

2. Genetic Algorithm for VLSI Design, Layout and Test Automation - PinakiMazumder, E.Mrudnick, Prentice Hall,1998.

3. Convex Optimization - Stephen Boyd, LievenVandenberghe, Cambridge University Press,2004.

M Tech 1st SEMESTER	L	P	C
	3	0	3
24VL1E04 :: CPLD and FPGA Architectures and Applications (ELECTIVE-II)			

UNIT-I: Introduction to Programmable Logic Devices
Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II: Field Programmable Gate Arrays
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT-III: SRAM Programmable FPGAs
Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT-IV: Anti-Fuse Programmed FPGAs
Introduction, Programming Technology, DeviceArchitecture,TheActelACT1,ACT2andACT3 Architectures.

UNIT-V: Design Applications
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design -CharlesH.RothJr, Lizy Kurian John, Cengage Learning.

REFERENCEBOOKS:

1. Field Programmable Gate Arrays-JohnV. Oldfield, Richard C.Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays- K.Chan/SamihaMourad,Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs- Ian Grout, Elsevier, Newnes.
4. 4.FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

M Tech 1st SEMESTER	L	P	C
	3	0	3
24VL1E05 :: Advanced Computer Architecture (ELECTIVE-II)			

UNIT-I: Fundamentals of Computer Design

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, Operations in the instruction set.

UNIT-II:

Pipelines

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design

Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT-III:

Instruction Level Parallelism (ILP)-The Hardware Approach

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach

Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT-IV:

Multi Processors and Thread Level Parallelism

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT-V:

Inter Connection and Networks

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture

Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors

2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

3. Advanced Computer Architecture - A Design Space Approach, DezsoSima, Terence Fountain, Peter Kacsuk, Pearson Ed.

M Tech 1st SEMESTER	L	P	C
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24VL1E06 :: Hardware Software Co-Design (ELECTIVE-II)			

UNIT-I:

Co- Design Issues

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT-II:

Prototyping and Emulation

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III:

Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT-IV:

Design Specification and Verification

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT-V:

Languages for System-Level Specification and Design-I

System-level specification, design representation for system level synthesis, system level specification languages.

Languages for System-Level Specification and Design-II

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer Publications.

M Tech 1st SEMESTER	L	P	C
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24CC1T01 :: Research Methodology and IPR			

UNIT-I:

Meaning of research problem, Sources of research problem,Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II:

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT-III:

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-V:

Patent Rights: Scope of Patent Rights.Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc.Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science &engineering students""
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCES:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New TechnologicalAge", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

M Tech 1st SEMESTER	L	P	C
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CMOS System Design Using VHDL Laboratory			

List of Experiments

1. Develop VHDL Code For All Logic Gates using xillinx and simulate the results
2. Develop VHDL Code for priority encoder and simulate its results.
3. Develop VHDL Code for ones counter and simulate its results.
4. Develop VHDL Code for single port synchronous.
5. Develop VHDL Code for ALU and Simulate it results.
6. Develop VHDL Code for pattern detection using Moore machine.
7. Develop VHDL Code for Finite State Machine (FSM) based logic circuit.
8. Develop VHDL Code for parity generator and Simulate it results.
9. Write VHDL Code for traffic light control and Simulate it results.
10. Develop VHDL Code for clock divider and Simulate it results.

Software required:

1. **Xilinx ISE 9.1**

M Tech 1st SEMESTER	L	P	C
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CMOS Layout Design Laboratory			

List of Experiments

1. Introduction to Micro wind and analysis of CMOS 0.25 micron technology MOSFET'S
2. Layout of Basic Gates and complex circuit using CMOS 0.25micronTechnology in Micro wind.
3. Layout of XOR and XNOR Gates using CMOS0.25micron Technology in Micro wind.
4. Layout of Multiplexer usingCMOS0.25micronTechnologyin Micro wind.
5. Layout of De multiplexer using CMOS0.25micronTechnology in Micro wind.
6. Layout of Shifter using CMOS0.25micronTechnologyin Micro wind.
7. Design and implementation of Layout of Full Adder using CMOS0.25 micron Technology in Micro wind.
8. Design and implementationofLayoutof2-bitComparatorusing CMOS0.25micronTechnologyin Micro wind.
9. DesignandimplementationofLayoutof2-bitComparatorusing CMOS0.25micronTechnologyin Micro wind.
10. DesignandimplementationofLayoutof4x4bitMultiplier CMOS0.25micronTechnologyinMicrowind.
11. Design and implementation of Layout of RS-Latch in CMOS 0.25micronTechnologyinMicrowind.
12. Design and implementation of Layout of D Latch in CMOS 0.25micronTechnologyinMicrowind.
13. Design and implementation of Layout of Synchronous Counter in CMOS 0.25micronTechnology in Micro wind.
14. Design and implementation of Layout of Asynchronous Counter in CMOS0.25 micron Technology in Micro wind.

Software required:

1. **Micro wind**

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Audit Course-I			

M Tech 2st SEMESTER	L	P	C
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24VL2T01 :: Low Power VLSI Design			

UNIT-I: Fundamentals of Low Power VLSI Design

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT-II: Low-Power Design Approaches

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT-III: Low-Voltage Low-Power Adders

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT-IV: Low-Voltage Low-Power Multipliers

Introduction,Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT-V: Low-Voltage Low-Power Memories

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Pre charge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
2. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
3. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
4. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

M Tech 2st SEMESTER	L	P	C
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24VL2T02 Design for Testability			

UNIT-I: Introduction to Testing

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II: Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT -III:

Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV:

Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V:

Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Aggrawal, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

M Tech 2st SEMESTER	L	P	C
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24VL2E07 :: VLSI and NANO Material (ELECTIVE-III)			

UNIT I

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nano structures – precipitate – reactive– hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT II

Fundamentals of Nano materials, Classification, Zero-dimensional Nano materials, One-dimensional Nano materials, Two-dimensional Nano materials, Three dimensional Nano materials. Low-Dimensional Nano materials and its Applications, Synthesis, Properties, and applications of Low-Dimensional Carbon-Related Nano materials.

UNIT III

Micro- and Nanolithography Techniques, Emerging Applications Introduction to Micro electro Mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micro machining, Bulk Micro machining, Molding.Introduction to Nano Phonics.

UNIT IV

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT‟s - Multi-walled Nano tubes, Single-walled Nano tubes Optical properties ofCNT‟s, Electrical transport in perfect Nano tubes, Applications as case studies. Synthesis and applications of CNT's.

UNIT V

Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane based application, polymer based application.

Text Books:

1. Kenneth J. Klabunde and Ryan M. Richards, “Nano scale Materials in Chemistry”, 2nd edition,John Wiley and Sons, 2009.

2. I Gusev and A ARempel, “Nano crystalline Materials”, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.

3. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, “Nano science and Nanotechnology”, Tata McGraw Hill Education 2012

M Tech 2st SEMESTER	L	P	C
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24VL2E08 :: DSP Processors & Architectures (ELECTIVE-III)			

UNIT-I:

Introduction to Digital Signal Processing

Introduction to a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II:

Architectures for Programmable DSP Devices

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT-III:

Programmable Digital Signal Processors

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-IV:

Analog Devices Family of DSP Devices

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal

Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT-V:

Interfacing Memory and I/O Peripherals to Programmable DSP Devices

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-SengGan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications-B. Venkataramani and M. Bhaskar, 2002, TMH.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
3. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
4. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997

M Tech 2st SEMESTER	L	P	C
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24VL2E09 CAD for VLSI (ELECTIVE-III)			

UNIT-I: VLSI Physical Design Automation

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles

UNIT-II: Partitioning, Floor Planning, Pin Assignment and Placement

Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement **–** Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms;

UNIT-III: Global Routing and Detailed Routing

Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms;

UNIT-IV: Physical Design Automation of FPGAs and MCMs

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model;
Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT-V: Chip Input and Output Circuits

ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by NaveedShervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

M Tech 2st SEMESTER	L	P	C
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24VL2E10 :: System On Chip Design (ELECTIVE-IV)			

UNIT-I: Introduction to the System Approach

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II: Processors

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT-III: Memory Design for SOC

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV: Interconnect Customization and Configuration

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT-V: Application Studies / Case Studies

SOC Design approach,AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

M Tech 2st SEMESTER	L	P	C
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24VL2E11 :: CMOS Mixed Signal Design (ELECTIVE-IV)			

UNIT-I: Switched Capacitor Circuits

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-II: Phased Lock Loop (PLL)

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III: Data Converter Fundamentals

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV: Nyquist Rate A/D Converters

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT-V: Oversampling Converters

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizierss, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

M Tech 2st SEMESTER	L	P	C
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24VL2E12 :: ASIC Design and Development (ELECTIVE-IV)			

UNIT-I Introduction to embedded system design, Design issue in system development, Architecture of 8051 µc and its description, Pin diagram of 8051 µc and its description, addressing modes, instruction sets, Arithmetic and logical operation, Sub-router, Interrupt handling timing sub-router, Serial data transmission, Serial data communication

UNIT-II Introduction to ASIC, Types of ASIC, ASIC cell library, CMOS logic, CMOS Process, CMOS Design rule, Combinational logics, Combinational logics, Data path logic cell, Sequential logic cell, I/O cell, cell compiler

UNIT-III ASIC library cell design: Transistor and resistors, Transistor parasitic capacitance, Logical Effort, Library cell design, Library architecture, Gate array design, standard cell design, Programmable ASIC Design, Anti fuse, Static RAM, EPROM, EEPROM Technology

UNIT-IV Low level Design Entry, Schematic design Entry, Language, PLA, Tool, EDIF, Overview, Hardware descriptive language VHDL, Hardware descriptive language Verilog, Logic synthesis VHDL Simulation, Logic synthesis VHDL Simulation, Floor Planning

UNIT-V FPGA based system: Basic concept, Digital Design Digital Design and FPGA, FPGA Fabrics: FPGA architecture and its description Static RAM based FPGA, Permanent FPGA, Chip I/O, Circuit design of FPGA, Logic implementation of FPGA architecture

RECOMMENDED BOOKS: Text Books: 1. M J S Smith/ Application Specific Integration Circuit. Pearson Edu 2005

M Tech 2st SEMESTER	L	P	C
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24VL2L01:: System Verilog Programming Laboratory			

List of Experiments

1. Develop VERILOG Code For All Logic Gates using Xilinx and simulate the results
2. Develop VERILOG Code for priority encoder and simulate its results.
3. Develop VERILOG Code for ones counter and simulate its results.
4. Develop VERILOG Code for single port synchronous.
5. Develop VERILOG Code for ALU and Simulate it results.
6. Develop VERILOG Code for pattern detection using Moore machine.
7. Develop VERILOG Code for Finite State Machine (FSM) based logic circuit.
8. Develop VERILOG Code for parity generator and Simulate it results.
9. Develop VERILOG Code for traffic light control and Simulate it results.
10. Develop VERILOG Code for clock divider and Simulate it results.

M Tech 2st SEMESTER	L	P	C
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24VL2L02 :: CMOS Testing and Verification Laboratory			

1. Develop CMOS Inverter and their Test bench for Verification
2. Develop NOR gate and their Test bench for Verification
3. Develop XOR gate and their Test bench for Verification
4. Develop Transmission gate and their Test bench for Verification
5. Develop Sub tractor and their Test bench for Verification
6. Develop 2x4 Decoder and their Test bench for Verification
7. Develop 8x1 Multiplexer and their Test bench for Verification
8. Develop all types of Flip-flops and their Test benches for Verification
9. Develop Half adder and their Test bench for Verification
10. Develop Full adder and their Test bench for Verification

M Tech 2st SEMESTER	L	P	C
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24VL2P01 :: Technical Seminar			

M Tech 2st SEMESTER	L	P	C
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Audit Course-II			

M Tech 3st SEMESTER	L	P	C
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24VL3E13 :: CMOS Digital IC Design			

UNIT-I

MOS Design Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III

Sequential MOS Logic Circuits Behavior of bi stable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV

Dynamic Logic Circuits Basic principle, Voltage Boot strapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V

Semiconductor Memories Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

M Tech 3st SEMESTER	L	P	C
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24VL3E14 :: Semiconductor Memory Design and Testing			

UNIT-I: Random Access Memory Technologies

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II: Non-volatile Memories

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT-III: Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance

RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT-IV: Semiconductor Memory Reliability and Radiation Effects

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT-V: Advanced Memory Technologies and High-density Memory Packing Technologies

Ferroelectric RAMs (FRAMs),GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma-2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prent

M Tech 3st SEMESTER	L	P	C
	3	0	3
24VL3E15 :: VLSI Signal Processing			

UNIT-I:
Introduction to DSP
Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

Pipelining and Parallel Processing
Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power

Retiming
Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT-II:
Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT-III:
Systolic Architecture Design
Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT-IV:
Fast Convolution
Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT-V:
Low Power Design
Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches

Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

M Tech 3st SEMESTER	L	P	C
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24CM3O01 :: Business Analytics			

UNIT1:

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics.
Statistical Tools: Statistical Notation, Descriptive Statistical methods,
Review of probability distribution and data modeling, sampling and estimation methods overview.

UNIT 2:

Trendiness and Regression Analysis: Modeling Relationships and Trends in Data, simple Linear Regression, Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology

UNIT 3:

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modeling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modeling, nonlinear Optimization.

UNIT 4:

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.
Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation
Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT 5:

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, the Value of Information, Utility and Decision Making.
Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism

Reference:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

M Tech 3st SEMESTER	L	P	C
	3	0	3
24CM3O02 :: Industrial Safety			

UNIT-1:

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting,equipment and methods.

UNIT-2:

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT-3:

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT-4:

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment‟s like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine,v. Boiler,vi .Electrical motors, Types of faults in machine tools and their general causes.

UNIT-5:

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii.Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

REFERENCE:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman &Hall London

M Tech 3st SEMESTER	L	P	C
	3	0	3
24CM3O03 :: Operations Research			

UNIT 1:

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

UNIT 2

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

UNIT 3:

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

UNIT 4

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT 5

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

REFERENCES:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Liebermann Operations Research: McGraw Hill Pub. 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

M Tech 3st SEMESTER	L	P	C
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24CM3O04 :: Cost Management of Engineering Physics			

Introduction and Overview of the Strategic Cost Management Process

Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non- technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

REFERENCES:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

M Tech 3st SEMESTER	L	P	C
	3	0	3
24CM3O05 :: Composite Material			

UNIT–I:

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix.Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance

UNIT – II:

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT – III:

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT–IV:

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT – V:

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygro thermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TEXT BOOKS:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition,2007.

REFERENCES:

1. Hand Book of CompositeMaterials-ed-Lubin.
2. Composite Materials – K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L.Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi.

M Tech 3st SEMESTER	L	P	C
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24CM3O06 :: Waste to Energy			

UNIT-I:

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest esidue, Industrial waste - MSW – Conversion devices – Incinerators, gasifies, digesters

UNIT-II:

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyro lytic oils and gases, yields and applications.

UNIT-III:

Biomass Gasification: Gasifies – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifies burner arrangement for
thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation

UNIT-IV:

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT-V:

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

REFERENCES:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

M Tech 3st SEMESTER	L	P	C
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24LV3P01 Project Work Part-I			

M Tech 4st SEMESTER	L	P	C
	0	32	16
24VL4P02 Project Work Part-II			

Audit Course I & II
ENGLISH FOR RESEARCH PAPER WRITING

Course objectives: Students will be able to: Understand that how to improve your writing skills and level of readability Learn about what to write in each section Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission		
Syllabus		
Units	**CONTENTS**	**Hours**
1	Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness	4
2	Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction	4
3	Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.	4
4	key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,	4
5	skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions	4
6	useful phrases, how to ensure paper is as good as it could possibly be the first- time submission	4

SUGGESTED STUDIES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for MathematicalSciences,SIAM. Highman‟sbook .
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

Audit Course I & II
DISASTER MANAGEMENT

Course Objectives: -Students will be able to:

learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.

critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in

Syllabus

Units	CONTENTS	Hours
1	**Introduction** Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.	4
2	**Repercussions Of Disasters And Hazards**: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man- made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.	4
3	**Disaster Prone Areas In India** Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics	4
4	**Disaster Preparedness And Management** Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.	4
5	**Risk Assessment** Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People‟s Participation In Risk Assessment. Strategies for Survival.	4
6	**Disaster Mitigation** Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.	4

SUGGESTED READINGS:

1. R. Nishith, Singh AK, “Disaster Management in India: Perspectives, issues and strategies ““New Royal book Company.
2. Sahni, PardeepEt.Al. (Eds.),” Disaster Mitigation Experiences And Reflections”, Prentice Hall

Of India, New Delhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep &Deep Publication Pvt. Ltd., New Delhi.

Audit Course I & II
SANSKRIT FOR TECHNICAL KNOWLEDGE

COURSE OBJECTIVES

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning
3. Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
4. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient Literature

Syllabus

Unit	Content	Hours
1	• Alphabets in Sanskrit, • Past/Present/Future Tense, • Simple Sentences	8
2	• Order • Introduction of roots • Technical information about Sanskrit Literature	8
3	• Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics	8

SUGGESTED READING

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India‟s Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

COURSE OUTPUT

Students will be able to

1. Understanding basic Sanskrit language
2. Ancient Sanskrit literature about science & technology can be understood
3. Being a logical language will help to develop logic in students

Audit Course I & II
VALUE EDUCATION

COURSE OBJECTIVES

Students will be able to

1. Understand value of education and self- development
2. Imbibe good values in students
3. Let the should know about the importance of character

SYLLABUS

Unit	Content	Hours
1	• Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. • Moral and non- moral valuation. Standards and principles. • Value judgments	4
2	• Importance of cultivation of values. • Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. • Honesty, Humanity. Power of faith, National Unity. • Patriotism. Love for nature ,Discipline	6
3	• Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. • Punctuality, Love and Kindness. • Avoid fault Thinking. • Free from anger, Dignity of labor. • Universal brotherhood and religious tolerance. • True friendship. • Happiness Vs suffering, love for truth. • Aware of self-destructive habits. • Association and Cooperation. • Doing best for saving nature	6
4	• Character and Competence –Holy books vs Blind faith. • Self-management and Good health. • Science of reincarnation. • Equality, Nonviolence, Humility, Role of Women. • All religions and same message. • Mind your Mind, Self-control. • Honesty, Studying effectively	6

SUGGESTED READING

1 Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

COURSE OUTCOMES

1. Students will be able to 1.Knowledge of self-development
2. Learn the importance of Human values 3.Developing the overall personality

Audit Course I & II
CONSTITUTION OF INDIA

COURSE OBJECTIVES:

Students will be able to:

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opinion regarding modern Indian intellectuals‟ constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Units	Content	Hour s
1	**History of Making of the Indian Constitution:** History Drafting Committee, (Composition & Working)	4
2	**Philosophy of the Indian Constitution:** Preamble Salient Features	4
3	**Contours of Constitutional Rights & Duties:** Fundamental Rights Right to Equality Right to Freedom Right against Exploitation Right to Freedom of Religion Cultural and Educational Rights Right to Constitutional Remedies Directive Principles of State Policy Fundamental Duties.	4
4	**Organs of Governance:** Parliament Composition Qualifications and Disqualifications Powers and Functions Executive President Governor Council of Ministers Judiciary, Appointment and Transfer of Judges, Qualifications Powers and Functions	4
5	**Local Administration:** District‟s Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CE of Municipal Corporation. Pachayati raj: Introduction, PRI: ZilaPachayat. Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy	4
6	**Election Commission:** Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.	4

SUGGESTED READING

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

COURSE OUTCOMES:

Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

Audit Course I & II
PEDAGOGY STUDIES

Course Objectives:

Students will be able to:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

Syllabus		
Units	**Content**	**Hours**
1	**Introduction and Methodology:** • Aims and rationale, Policy background, Conceptual framework and terminology • Theories of learning, Curriculum, Teacher education. • Conceptual framework, Research questions**.** • Overview of methodology and Searching.	4
2	• Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. • Curriculum, Teacher education.	2
3	• Evidence on the effectiveness of pedagogical practices • Methodology for the in depth stage: quality assessment of included studies. • How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? • Theory of change. • Strength and nature of the body of evidence for effective pedagogical practices. • Pedagogic theory and pedagogical approaches. • Teachers‟ attitudes and beliefs and Pedagogic strategies.	4
4	• Professional development: alignment with classroom practices and follow-up support • Peer support • Support from the head teacher and the community. • Curriculum and assessment • Barriers to learning: limited resources and large class sizes	4
5	**Research gaps and future directions** • Research design • Contexts • Pedagogy • Teacher education • Curriculum and assessment • Dissemination and research impact.	2

SUGGESTED READING

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education

research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, „learning to read" campaign. www.pratham.org/images/resource%20working%20paper%202.pdf.

COURSE OUTCOMES:

Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

Audit Course I & II
STRESS MANAGEMENT BY YOGA

Course Objectives

1. To achieve overall health of body and mind
2. To overcome stress

Syllabus

Unit	Content	Hours
1	• Definitions of Eight parts of yog. (Ashtanga)	8
2	Yam and Niyam. Do`s and Don‟t‟s in life. i) Ahinsa, satya, astheya, bramhacharya and aparigraha ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan	8
3	• Asan and Pranayam 1. Various yog poses and their benefits for mind & body 2. Regularization of breathing techniques and its effects-Types of pranayama	8

SUGGESTED READING

1. Yogic Asanas for Group Tarining-Part-I : Janardan Swami Yogabhyasi Mandal, Nagpur
2. “Rajayoga or conquering the Internal Nature” by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

COURSE OUTCOMES:

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

Audit Course I & II

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

COURSE OBJECTIVES

To learn to achieve the highest goal happily

To become a person with stable mind, pleasing personality and determination

To awaken wisdom in students

SYLLABUS

Unit	Content	Hours
1	Neetisatakam-Holistic development of personality • Verses- 19,20,21,22 (wisdom) • Verses- 29,31,32 (pride & heroism) • Verses- 26,28,63,65 (virtue) • Verses- 52,53,59 (dont‟s) • Verses- 71,73,75,78 (do‟s)	8
2	• Approach to day to day work and duties. • Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48, • Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35, • Chapter 18-Verses 45, 46, 48.	8
3	• Statements of basic knowledge. • Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 • Chapter 12 -Verses 13, 14, 15, 16,17, 18 • Personality of Role model. Shrimad Bhagwad Geeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42, • Chapter 4-Verses 18, 38,39 • Chapter18 – Verses 37,38,63	8

SUGGESTED READING

1. “Srimad Bhagavad Gita” by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari‟s Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

COURSE OUTCOMES

Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students