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| **S NO** | **QUESTIONS** | **KNOWLEDGE**  **LEVEL** | **CO** |
| **UNIT -I** | | | |
| 1.a | Convert the following to decimal number system and then to binary number system.  i) (1416)H ii) (A41C)H iii) (7012)8 iv) (1212)10 | K2 | CO1 |
| 1.b | Explain about binary codes. | K2 | CO2 |
| 2.a | Write the dual and complement of the following.  i) Y=A’BD+ABD’+A(B’D’+C)  ii) Y=X’YZ+XY+XY’Z’+X’Y’ | K3 | CO2 |
| 2.b | Construct a logic circuit using minimum number of basic gates  i) Y=AB+A(B+C)+B’(A+D)  ii) Y=ABEF+AB(EF)’+(AB)’EF | K3 | CO2 |
| 3.a | Express the decimal digits 0-9 in BCD, 8-4-2-1, Excess-3, 2-4-2-1 codes? | K2 | CO1 |
| 3.b | List the first 20 numbers in base 13. Use the letters A,B,C to represent the last three digits. | K1 | CO1 |
| **UNIT -2** | | | |
| 1 | Construct a logic circuit using minimum number of NAND gates for the following expression.  Y=(A+B’+C)(A’+B’+C’)(A’+D’)(A’+B+C+D) | K3 | CO3 |
| 2 | Construct a logic circuit using minimum number of NOR gates for the following expression.  Y=AB(CD)’+AC(BD)’+ABCD+(BD)’(AC)’ | K3 | CO3 |
| 3 | Discover the minimal SOP expression for the following Boolean expression.  F(A,B,C,D,E)= ∑m(5,11,13,15,16,24,25,28,29,31) + ∑d(0,4,7,8,14,27). | K1 | CO2 |
| **UNIT -3** | | | |
| 1 | Explain about Decoders and design 2-to-4 decoder. | K2 | CO3 |
| 2 | Explain about Decoders and design 3-to-8 decoder. | K2 | CO3 |
| 3 | Explain design procedure of the combinational logic circuits and design full adder. | K3 | CO3 |
| **UNIT -4** | | | |
| **1** | Explain the procedure for the design of combinational circuits with examples. | K2 | CO3 |
| **2** | Explain Universal shift register with neat diagram. | K3 | CO3 |
| **3** | Explain negative edge triggered D flip flop and give the timing diagram. | K2 | CO3 |
| **UNIT- 5** | | | |
| **1** | Compare Synchronous and Asynchronous counters. | K2 | CO3 |
| **2** | Explain four bit Ring counter and Johnsons counter | K4 | CO3 |
| **3** | Explain Synchronous and Asynchronous Counters. Compare their merits and demerits. | K3,K2 | CO3 |
| **UNIT 6** | | | |
| **1** | Compare CPLD and FPGA. | K2 | CO4 |
| **2** | Construct a logic circuit using PAL for the following Boolean functions.  i) w(A,B,C,D)=∑m(0,2,6,7,8,9,12,13)  ii) x(A,B,C,D)=∑m(0,2,6,7,8,9,12,13,14)  iii)y(A,B,C,D)=∑m(2,3,8,9,10,12,13)  iv)z(A,B,C,D)=∑m(1,3,4,6,9,12,14) | K3 | CO4 |
| **3** | Construct a combinational circuit using a ROM, the circuit accepts a Three bit number and generates an output binary number equal to their corresponding Excess- 3 code. | K3 | CO4 |