

COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

Accredited by National Board of Accreditation, AICTE, New Delhi, Accredited by NAAC with "A" Grade – 3.32 CGPA, Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi, Permanent Affiliation to JNTUK, Kakinada Seetharampuram, W.G.DT., Narsapur-534280, (Andhra Pradesh)

DEPARTMENT OF ARTIFICIAL INTELLIGENCE & DATA SCIENCE

TEACHING PLAN

			Course Semes Branches Title ter		Contact Periods /Week	SWEET,	lemic ear	Date of commence ment of Semester		
20CS3T03 ORGA		MPUTEI ANIZATI AND HTECTU	ON III	CSE AIDS	5	2023	3-24	07/08/2023		
Pre-r	equisites:		Basics o	of Computer Ha	rdare					
COU	RSE OUTCO	MES	L.							
			ure of computer	organization and	d its instructi	on sets.(K	(1,K2)			
				nd language concepts.(K1)						
3	Explain the arit	hmetic al	gorithms and de	ams and decimal arithmetic operations .(K1,K2,K3)						
4	Demonstrate input/output and		t and memory o	memory organization in the computer systems.(K2,K3)						
5	Express the cor	ncept of p	ipelining and va	rious processor	families.(K2	K6)	- 1-			
Unit Out Comes / Bloom's Level		Topics No.	Т	opics/Activity		Text Book / Refere nce	Cont act Hour	Method		
	20.01		UNI	T-I: Introduct	ion					
		-	Basic Structur Machine Instr	re of Computer ructions	s and					
	CO1:	1.01	Basic Organiza	ation of Compute	ers	T2	1	Chalk ,talk		
	Describe the basic	1.02	Von Newmann	Computers		Т2	1	Chalk ,talk		
I	structure of computer	1.03	Functional Uni	its		T2	1	Chalk ,talk		
	organizatio	1.04	Basic Operatio	nal Concepts,		T2	1	Chalk ,talk		
	n and its	1.05	Generation of	computers		T2	1	PPT		
	instruction	1.06	Numbers			T2	1	PPT		
	sets.(K1,K2)	1.07		erations and Inst		T2	1	PPT		
		1.08		tions and Addres		T2	1	Chalk ,talk		
		1.09	Instructions an	d Instruction Se	quencing	T2	1	PPT		



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		1.10	Addressing Modes	T2	1	Chalk, Talk,PPT
	1.11		Assembly Language	T2	1	PPT
	1.12		Basic Input / Output Operations	T2	1	PPT
		1.13	Case study: Arithmetic & Logic Instructions of ARM Processor	T1	1	Web Resources
		1.14	Branch Instructions of ARM Processor	T1	1	Web Resources
		1.15	I/O Operations of ARM Processor	T 1	1	Web Resources
			Total		15	
			UNIT-II: Stacks and Queues			
			Central Processing Unit and Programming the basic Computer			
		2.01	CPU - General Register and Stack Organizations	T2	1	Chalk ,Talk
		2.02	Instructions Formats	T2	1	Web Resources
	CO2:	2.03	Addressing Modes	T2	1	Chalk ,Talk
	Define the	2.04	Data Transferand Manipulation	T2	1	Chalk ,Talk
II	CPU operations and language	2.05	RISC	T2	1	Web Resources
11		2.06	Programming the Basic Computer – Machine Language	T2	1	Web Resources
	concepts.(K	2.07	Assembly Language	T2	1	Chalk ,Talk ,PPT
	-	2.08	Programming Arithmetic Operations	T2	1	PPT
		2.09	Programming Logic Operations		1	
		2.10	Micro Program Examples	T2	1	Web Resources
		2.11	Case Study – Design of Control Unit.	T2	1	Web Resources
	10.		Total			11
	to an arms of the second		UNIT-III: Linked Lists			
	CO3:		Computer Arithmetic			
	Explain the	3.0		T2	1	Chalk ,Talk
	arithmetic	3.02	Addition with Signed-2' Complement Data	T2	1	Chalk ,Talk
III	algorithms and	3.03	Subtraction with Signed-Magnitude Data	T2	1	Chalk ,Talk, PPT
	decimal arithmetic	3.04		T2	1	Chalk ,Talk
	operations .(K1,K2,K3)	3.03	Multiplication Algorithms:Hardware Implementation for Signed-Magnitude	T2	1	Chalk ,Talk



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		3.06	Booth Multiplication Algorithm	T2	1	
	,	3.07	Division Algorithms	T2	1	Chalk ,Talk,PPT
		3.08	Floating Point Arithmetic operations	T2	1	PPT
		3.09	Decimal Arithmetic Unit	T2	1	PPT
		3.10	Decimal Arithmetic Operations	T2	1	Web Resources
				Total		10
		UNIT-	IV: Input-Output and Memory Organ	ization		
		4.01	Accessing I/O Devices	T2	1	PPT
	004	4.02	Interrupts	T2	1	Chalk ,Talk
	CO4:	4.03	Direct Memory Access	T2	1	Chalk ,Talk
	Demonstrat	4.04	Buses	T2	1	PPT
IV	e	4.05	Interface Circuits	T2	1	Chalk ,Talk
	input/outp	4.06	Standard I/O interfaces	T2	1	Chalk ,Talk
	ut and	4.07	Memory Hierarchy	T2	1	Chalk ,Talk
	memory	4.08	Processor Examples Memory	T2	-	Web
	organizatio		Hierarchy		1	Resources
	n in the computer	4.09	Main Memory	T2	1	Chalk ,Talk,PPT
	systems.(K2	4.10	Auxiliary Memory	T2	1	Chalk ,Talk
100	,K3)	4.11	Associative Memory	T2	1	Chalk ,Talk
		4.12	Virtual Memory	T2		PPT
	Re	vision Dir	rect Memory Access		1	Chalk ,Talk PPT
		***************************************		Total		13
		UN	NIT-V: Pipelining and Processor Fami	lies		
		5.01	Basic Concepts	T2,T1	1	Web Resources
	CO5: Express the concept of	5.02	Data Hazards	T2,T1	1	Web Resources, Chalk,talk
V	pipelining	5.03	Instruction Hazards	T2,T1	1	Chalk ,talk ppt
	and various	5.04	Influence on Instruction sets	T2,T1	1	PPT
	processor families.(K2	5.05		T2,T1	1	Web Resources
	TOTAL STREET,		Consideration			
	,K6)	5.06		T2,T1	1	Chalk ,Tall



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5.09 Motorola 680X0 and Coldfire T1,R1 1 Web Resources		5.08	ARM family	T1,R1	1	Web Resources
SPARC Family		5.09		T1,R1	1	
Discussion of previous year question papers Total Discussion of previous papers Total Discussion of previous papers Total Discussion of previous year question papers Total Discussion of previous papers Total Discussion of papers D		5.10	Intel IA 64 Family	T1,R1	1	Web Resources
Discussion of previous year question papers Total Discussion of previous papers Total Discussion of previous year question papers Total Discussion of previous year question papers Total Discussion of previous peacetopapers Total Discussion of previous papers Total Discussion of papers Total Discussion of papers Total Discussion of papers Total Discussion of pervicus papers Total Discussion of pervicus papers Tota		5.11	SPARC Family.	T1,R1	1	Web Resources
Discussion of previous year question papers Total CUMULATIVE PROPOSED PERIODS 65 Text Books: S.No. AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION Carl Hamacher, Zvonks Varanesic ,SafeaZaky,Computer Organization,Fifth Edition McGraw Hill 2015. M. Moris Mano ,Computer System Organization, Pearson PTE academic Revised Thir Edition 2019. Reference Books: S.No. AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION William Stallings ,Computer Organization and Architecture,Sixth Edition, Pearson/PHI 2006 John L. Hennessy and David A. Patterson Computer Organization a quantitative approach Fourth Edition, Elsevier 2012. Andrew s. Tanenbaum ,Structured Computer Organization -4th Edition, PHI/ Pearson 2012 Andrew s. Tanenbaum ,Structured Computer Organization and Design,Springer Intellition-2014. Web Details https://en.wikibooks.org/wiki/IB/Group 4/Computer Science/Computer Organisation					1	
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3	http://www.cse.iitm.ac.in/~vplab/courses/comp_org.html

		Name	Signature with Date
i.	Faculty	Mr.K, Satya Narayana	
iii.	Course Coordinator	Dr. G Sudha kar	J.Cg
iv.	Module Coordinator	Dr. B Rama krishna	BB

Principal