SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

Accredited by National Board of Accreditation, AICTE, New Delhi,Accredited by NAAC with "A" Grade – 3.32 CGPA,Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi,Permanent Affiliation to JNTUK, Kakinada
Seetharampuram, W.G.DT., Narsapur-534280, (Andhra Pradesh)

DEPARTMENT OF ARTIFICIAL INTELLIGENCE & DATA SCIENCE

TEACHING PLAN

Course Code	Course Title	Semester	Branches	Contact Periods /Week	Academic Year	Date of commencement of Semester
20CS3T03	COMPUTER ORGANIZATION AND ARCHITECTURE	III	CSE AIDS	5	2023-24	07/08/2023

Pre-requisites:	Basics of Computer Hardare

COURSE OUTCOMES

1	Describe the basic structure of computer organization and its instruction sets.(K1,K2)
2	Define the CPU operations and language concepts.(K1)
3	Explain the arithmetic algorithms and decimal arithmetic operations .(K1,K2,K3)
4	Demonstrate input/output and memory organization in the computer systems.(K2,K3)
5	Express the concept of pipelining and various processor families.(K2,K6)

Unit	Out Comes / Bloom's Level	Topics No.	Topics/Activity	Text Book / Reference	Contact Hour	Delivery Method
UNIT-I: Introduction						
I	CO1: Describe the basic structure of computer organization and its instruction sets.(K1,K2)		**Basic Structure of Computers and Machine Instructions**			
		1.01	Basic Organization of Computers	T2	1	Chalk ,talk
		1.02	Von Newmann Computers	T2	1	Chalk ,talk
		1.03	Functional Units	T2	1	Chalk ,talk
		1.04	Basic Operational Concepts,	T2	1	Chalk ,talk
		1.05	Generation of computers	T2	1	PPT
		1.06	Numbers	T2	1	PPT
		1.07	Arithmetic Operations and Instructions	T2	1	PPT
		1.08	Memory Locations and Addresses	T2	1	Chalk ,talk
		1.09	Instructions and Instruction Sequencing	T2	1	PPT

		1.10	Addressing Modes	T2	1	Chalk, Talk,PPT
		1.11	Assembly Language	T2	1	PPT
		1.12	Basic Input / Output Operations	T2	1	PPT
		1.13	Case study: Arithmetic & Logic Instructions of ARM Processor	**T1**	1	Web Resources
		1.14	Branch Instructions of ARM Processor	**T1**	1	Web Resources
		1.15	I/O Operations of ARM Processor	**T1**	1	Web Resources
				Total		**15**
UNIT-II: Stacks and Queues						
II	CO2: Define the CPU operations and language concepts.(K 1)		**Central Processing Unit and Programming the basic Computer**			
		2.01	CPU - General Register and Stack Organizations	T2	1	Chalk ,Talk
		2.02	Instructions Formats	T2	1	Web Resources
		2.03	Addressing Modes	T2	1	Chalk ,Talk
		2.04	Data Transferand Manipulation	T2	1	Chalk ,Talk
		2.05	RISC	T2	1	Web Resources
		2.06	Programming the Basic Computer – Machine Language	T2	1	Web Resources
		2.07	Assembly Language	T2	1	Chalk ,Talk ,PPT
		2.08	Programming Arithmetic Operations	T2	1	PPT
		2.09	Programming Logic Operations		1	
		2.10	Micro Program Examples	T2	1	Web Resources
		2.11	Case Study – Design of Control Unit.	T2	1	Web Resources
			Total			**11**
UNIT-III: Linked Lists						
III	CO3: Explain the arithmetic algorithms and decimal arithmetic operations .(K1,K2,K3)		**Computer Arithmetic**			
		3.01	Addition with Signed-Magnitude Data	T2	1	Chalk ,Talk
		3.02	Addition with Signed-2' Complement Data	T2	1	Chalk ,Talk
		3.03	Subtraction with Signed-Magnitude Data	T2	1	Chalk ,Talk, PPT
		3.04	Subtraction with Signed-2' Complement Data	T2	1	Chalk ,Talk
		3.05	Multiplication Algorithms:Hardware Implementation for Signed-Magnitude	T2	1	Chalk ,Talk

			Data			
		3.06	Booth Multiplication Algorithm	T2	1	
		3.07	Division Algorithms	T2	1	Chalk ,Talk,PPT
		3.08	Floating Point Arithmetic operations	T2	1	PPT
		3.09	Decimal Arithmetic Unit	T2	1	PPT
		3.10	Decimal Arithmetic Operations	T2	1	Web Resources
				Total	**10**	
UNIT-IV: Input-Output and Memory Organization						
IV	CO4: Demonstrate input/output and memory organization in the computer systems.(K2 ,K3)	4.01	Accessing I/O Devices	T2	1	PPT
		4.02	Interrupts	T2	1	Chalk ,Talk
		4.03	Direct Memory Access	T2	1	Chalk ,Talk
		4.04	Buses	T2	1	PPT
		4.05	Interface Circuits	T2	1	Chalk ,Talk
		4.06	Standard I/O interfaces	T2	1	Chalk ,Talk
		4.07	Memory Hierarchy	T2	1	Chalk ,Talk
		4.08	Processor Examples Memory Hierarchy	T2	1	Web Resources
		4.09	Main Memory	T2	1	Chalk ,Talk,PPT
		4.10	Auxiliary Memory	T2	1	Chalk ,Talk
		4.11	Associative Memory	T2	1	Chalk ,Talk
		4.12	Virtual Memory	T2		PPT
			Revision Direct Memory Access		1	Chalk ,Talk, PPT
				Total	**13**	
UNIT-V: Pipelining and Processor Families						
V	CO5: Express the concept of pipelining and various processor families.(K2 ,K6)	5.01	Basic Concepts	T2,T1	1	Web Resources
		5.02	Data Hazards	T2,T1	1	Web Resources, Chalk ,talk
		5.03	Instruction Hazards	T2,T1	1	Chalk ,talk, ppt
		5.04	Influence on Instruction sets	T2,T1	1	PPT
		5.05	Data Path and control consideration	T2,T1	1	Web Resources
		5.06	Superscalar Operation	T2,T1	1	Chalk ,Talk
		5.07	Performance Considerations	T2,T1	1	PPT

		5.08	ARM family	T1,R1	1	Web Resources
		5.09	Motorola 680X0 and Coldfire families	T1,R1	1	Web Resources
		5.10	Intel IA 64 Family	T1,R1	1	Web Resources
		5.11	SPARC Family.	T1,R1	1	Web Resources
Discussion of previous year question papers					1	
Discussion of previous year question papers					1	
Discussion of previous year question papers					1	
Discussion of previous year question papers					1	
Discussion of previous year question papers					1	
				Total	**16**	
				CUMULATIVE PROPOSED PERIODS	**65**	

Text Books:

S.No.	AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION
1	Carl Hamacher, Zvonks Varanesic ,SafeaZaky,Computer Organization,Fifth Edition, McGraw Hill 2015.
2	M. Moris Mano ,Computer System Organization, Pearson PTE academic Revised Third Edition 2019.

Reference Books:

S.No.	AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION
1	William Stallings ,Computer Organization and Architecture,Sixth Edition, Pearson/PHI. 2006
2	John L. Hennessy and David A. Patterson Computer Organization a quantitative approach, Fourth Edition, Elsevier 2012.
3	Andrew s. Tanenbaum ,Structured Computer Organization -4th Edition, PHI/ Pearson.-2012
4	Sivaraama, Dandamudi ,Fundamentals of Computer Organization and Design,Springer Int. Edition-2014.

Web Details

1	https://en.wikibooks.org/wiki/IB/Group_4/Computer_Science/Computer_Organisation
2	http://www.cs.uwm.edu/classes/cs458/Lecture/HTML/ch05.html

3	http://www.cse.iitm.ac.in/~vplab/courses/comp_org.html

		Name	Signature with Date
i.	Faculty	Mr.K.Satya Narayana	
iii.	Course Coordinator	Dr. G Sudha kar	
iv.	Module Coordinator	Dr. B Rama krishna	6/10/23

Principal