SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous)
SEETHARAMAPURAM, NARSAPUR-534280 W.G.DT. AP

DEPARTMENT OF BACHELOR OF COMPUTER APPLICATIONS(Honours)

TEACHING PLAN

Course Code	Course Title	Year/Sem	Branch	Contact hr/week	Academic Year
24BC2T04	Computer Organization	I/II	BCA(Honours)	6	2024-2025

Course Objectives:

The purpose of the course is to introduce principles of computer organization and the basic architectural concepts. It provides an in depth understanding of basic organization, design, programming of a simple digital computer, computer arithmetic, instruction set design, micro programmed control unit, pipelining and vector processing, memory organization and I/O systems.

Course Outcome(co's) : At the end of the course, student will be able to:

CO No.	Course Outcome	Knowledge Level (K)
CO1	Understand the basic structure of computers, including types, functional units, bus structures, software, performance factors, and data representation methods such as fixed-point and floating-point.	K2
CO2	Apply register transfer language to describe micro-operations including arithmetic, logic, and shift operations, and understand instruction codes, computer registers, and instruction cycles.	K3
CO3	Understand micro programmed control mechanisms and the organization of the central processing unit, including instruction formats, addressing modes, and data manipulation.	K4
CO4	Analyze different types of memory organization, including memory hierarchy, main memory, cache memory, and virtual memory, and understand concepts related to shift registers and RAID.	K4
CO5	Understand the organization of input-output systems, including peripheral devices, interfaces, data transfer modes, priority interrupts, DMA, and serial communication.	K2

Week No	Outcome	Blooms Level		Topic / Activity	Text Books	Contact Hours	Delivery Method
				UNIT-I			
1,2	Understand the basic structure of computers, including types, functional units, bus structures, software, performance factors, and data representation methods such as fixed-point and floating-point.	K2	1.1	Basic Structure Of Computers: Computer Types,	T1	1	Chalk & Board, PPT, Interactive Whiteboarding
			1.2	Functional unit,	T1	1	
			1.3	Basic Operational concepts, Bus structures,	T1	2	
			1.4	Software, Performance,	T1	2	
			1.5	multiprocessors and multi computers.	T1	2	
			1.6	Data Representation.	T1	1	
			1.7	Fixed Point Representation.	T1	2	
			1.8	Floating – Point Representation.	T1	2	
				UNIT-II			
3,4	Apply register transfer languageto describe micro-operations including arithmetic, logic,and shift operations, and understand instruction codes, computer registers, and instruction cycles.	K3	2.1	Register Transfer Language And Micro operations: Register Transfer language.	T1	2	Chalk & Board, PPT , Interactive Whiteboarding
			2.2	Register Transfer Bus and memory transfers,	T1	3	
			2.3	Arithmetic Micro operations,Logic, shift micro operations,	T1	3	
			2.4	Arithmetic logic shift unit. Instruction codes. ComputerRegisters Computer,instructions, Instruction cycle.	T1	4	
				Mid I Exam			

UNIT-III							
5, 6	Understand micro programmed control mechanisms and the organization of the central processing unit,including instruction formats, addressing modes, and data manipulation.	K4	3.1	Micro Programmed Control: Control memory,	T1	1	Chalk & Board, PPT , Interactive Whiteboarding
			3.2	Address sequencing, micro program example,	T1	2	
			3.3	design of control unit.	T1	2	
			3.4	Central Processing Unit: General Register Organization, Instruction Formats,	T1	3	
			3.5	Addressing modes, Data Transfer and Manipulation, Program Control.	T1	4	
UNIT-IV							
7,8	Analyze different types of memory organization, including memory hierarchy, main memory, cache memory, and virtual memory, and understand concepts related to shift registers and RAID.	K4	4.1	Memory Organization: Memory Hierarchy,	T1	2	Chalk & Board, PPT , Interactive Whiteboarding
			4.2	Main Memory,	T1	2	
			4.3	Auxiliary memory,	T1	2	
			4.4	Associate Memory, CacheMemory, Cache memories performance considerations,	T1	4	
			4.5	Virtual memories Introduction to Shift registers and RAID	T1	3	
UNIT-V							
9, 10	Understand the organization of input-output systems, including peripheral devices, interfaces, data transfer modes,	K3	5.1	Input–Output Organization: Peripheral Devices,	T1	3	Chalk & Board, PPT , Interactive Whiteboarding
			5.2	Input-Output Interface,	T1	2	
			5.3	Asynchronous data transfer, Modes of Transfer,	T1	4	

	priority interrupts, DMA, and serial communication .		5.4	Priority Interrupts, DMA, Input Output Processor, Serial Communication.	T1	4	
Mid II Exam							
Total No. of Classes						**63**	

Recommended Text Books for Reading:

Text Book 1 : Digital Logic and Computer Design,Moriss Mano, 11th Edition, Pearson Education.

Text Book 2 : Computer Organization,5thed.,Hamacher,Vranesicand Zaky,TMH,2002

Text Book 3 : Computer System Architecture, 3/e, Moris Mano, Pearson/PHI.

References Books:

1. Computer System Organization &Architecture, John D. Carpinelli, Pearson, 2008

2. Computer System Organization, Naresh Jotwani, TMH, 2009

3. Computer Organization &Architecture: Designing for Performance, 7thed., William Stallings, PHI, 2006

4. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson

Faculty Y. Sai Swaroopa

Head of the Department

Principal