



SWARNANDHRA COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

Accredited by National Board of Accreditation, AICTE, New Delhi, Accredited by
NAAC with "A" Grade – 3.32 CGPA, Recognized under 2(f) & 12(B) of UGC Act 1956,
Approved by AICTE, New Delhi, Permanent Affiliation to JNTUK, Kakinada
Sectharampuram, W.G.D.T., Narsapur-534280, (Andhra Pradesh)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING TEACHING PLAN

| Course Code | Course Title | Semester | Branches | Contact Periods /Week | Academic Year | Date of commencement of Semester | |
|---|--|---|--|-----------------------|---------------|----------------------------------|------------------------------|
| 20EC6T01 | MICROPROCESSORS & MICROCONTROLLERS | VI | ECE | 5 | 2024-2025 | 18-11-2024 | |
| COURSE OUTCOMES | | | | | | | |
| After completion of the course students are able to | | | | | | | |
| CO1 | Demonstrate architecture, instructions and addressing modes of 8086 Microprocessor (K3) | | | | | | |
| CO2 | Analyze 8086 interfacing with different peripherals and implement programs (K4) | | | | | | |
| CO3 | Examine 8051 Microcontroller interfacing and implement programs (K3) | | | | | | |
| CO4 | Sketch the architecture and applications of advanced processors (K3) | | | | | | |
| UNIT | Out Comes / Bloom's Level | Topics No. | Topics/Activity | Text Book / Reference | Contact Hour | Delivery Method | |
| I | CO1: Demonstrate architecture, instructions and addressing modes of 8086 Microprocessor (K3) | UNIT-1: INTRODUCTION ,8086 MICROPROCESSORS | | | | | Chalk & Talk, PPT & Tutorial |
| | | 1.1 | Basic Microprocessor Architecture & Family of Intel processors | T1,R1 | 1 | | |
| | | 1.2 | Little Endian and Big Endian Formats Von-Neumann and Harvard architectures RISC Vs CISC processors | T1,R1 | 1 | | |
| | | 1.3 | 8086 Microprocessor feature & Architecture | T1,R1 | 1 | | |
| | | 1.4 | Register organization | T1,R1 | 1 | | |
| | | 1.5 | Pin diagram/description | T1,R1 | 1 | | |
| | | 1.6 | Memory Segmentation | T1,R1 | 1 | | |
| | | 1.7 | Memory Address | T1,R1 | 1 | | |
| | | 1.8 | Physical memory organization | T1,R1 | 1 | | |
| | | 1.9 | Interrupt and interrupt | T1,R1 | 1 | | |



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| | | | | | | |
|------------|---|---------------------------------|--|--------------|----------------------|------------------------------|
| | | | response | | | |
| | | 1.10 | Minimum Mode configuration & system timings | T1,R1 | 1 | |
| | | 1.11 | Maximum Mode configuration | T1,R1 | 1 | |
| | | CLASS TEST | | | | 1 |
| | | | | Total | 12 | |
| II | CO1: Demonstrate architecture, instructions and addressing modes of 8086 Microprocessor (K3) | UNIT-2: 8086 PROGRAMMING | | | | Chalk & Talk, PPT & Tutorial |
| | | 2.1 | Program Development steps | T1,R1 | 1 | |
| | | 2.2 | Addressing modes of 8086 | T1,R1 | 1 | |
| | | 2.3 | Instruction set of 8086 | T1,R1 | 1 | |
| | | 2.4 | Instruction set of 8086 | T1,R1 | 1 | |
| | | 2.5 | Assembler directives | T1,R1 | 1 | |
| | | 2.6 | Assembler directives | T1,R1 | 1 | |
| | | 2.7 | Procedures | T1,R1 | 1 | |
| | | 2.8 | Macros | T1,R1 | 1 | |
| | | 2.9 | Assembly language programming | T1,R1 | 1 | |
| | | 2.10 | Programming development tools | T1,R1 | 1 | |
| | | CLASS TEST | | | | |
| | | | | Total | 11 | |
| III | CO2: Analyze 8086 interfacing with different peripherals and implement programs (K4) | UNIT-3: 8086 INTERFACING | | | | Chalk & Talk, PPT & Tutorial |
| | | 3.1 | 8255-PPI | T1,R1 | 1 | |
| | | 3.2 | 8255 Architecture | T1,R1 | 1 | |
| | | 3.3 | Interfacing switches and LEDs | T1,R1 | 1 | |
| | | 3.4 | Interfacing of seven segment display | T1,R1 | 1 | |
| | | 3.5 | Software and Hard ware interrupts | T1,R1 | 1 | |
| | | 3.6 | Intel 8251USART | T1,R1 | 1 | |
| | | 3.7 | Architecture and interfacing 8237 DMA controller | T1,R1 | 1 | |
| | | 3.8 | Stepper motor interfacing | T1,R1 | 1 | |
| | | 3.9 | Interfacing to D/A converters VFE | T1,R1 | 1 | |
| 3.10 | Interfacing to A/D | T1,R1 | 1 | | | |
| | | | | | Simulation exercises | |



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| | | converters | | | |
|---|--|------------|--|------------|----|
| | | CLAS TEST | | | 1 |
| | | | | Total | 11 |
| UNIT-4: 8051 MIROCONTROLLERS | | | | | |
| IV | CO3: Examine 8051 Microcontroller interfacing and implement programs (K3) | 4.1 | 8051 microcontroller Architecture | T2,R2 | 1 |
| | | 4.2 | 8051 pin description & I/O ports | T2,R2 | 1 |
| | | 4.3 | Memory organization | T2,R2 | 1 |
| | | 4.4 | Interrupts | T2,R2 | 1 |
| | | 4.5 | Timers | T2,R2 | 1 |
| | | 4.6 | Serial port | T2,R2 | 1 |
| | | 4.7 | Programming | T2,R2 | 1 |
| | | 4.8 | Instructions | T2,R2 | 1 |
| | | 4.9 | Addressing Modes | T2,R2 | 1 |
| | | 4.10 | Simple Programs | T2,R2 | 1 |
| | | 4.11 | Interfacing to D/A, A/D converters | T2,R2 | 1 |
| | | 4.12 | LCD interfacing | T2,R2 | 1 |
| | | | | CLASS TEST | |
| | | | | Total | 13 |
| UNIT-5: ADVANCED MICROPROCESSORS | | | | | |
| V | CO4: Sketch the architecture and applications of advanced processors (K3) | 5.25.1 | Introduction to ARM 16/32 bit processors | T3,R2 | 1 |
| | | 5.3 | ARM Architecture | T3,R2 | 1 |
| | | 5.4 | ARM organization | T3,R2 | 1 |
| | | 5.5 | Interrupt vector table | T3,R2 | 1 |
| | | 5.6 | Instruction set | T3,R2 | 1 |
| | | 5.7 | Data processing, load store instructions | T3,R2 | 1 |
| | | 5.8 | software interrupt instructions | T3,R2 | 1 |
| | | 5.9 | Program status register instructions, Loading, conditional execution | T3,R2 | 1 |
| | | 5.10 | Thumb programming model | T3,R2 | 1 |
| | | 5.11 | Thumb instruction set | T3,R2 | 1 |
| | | 5.12 | Intel Processors | T3,R2 | 1 |
| | | 5.13 | Pentium Processors | T3,R2 | 1 |
| | | 5.14 | i3 Processor | T3,R2 | 1 |



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|------------------------------------|-------------------------|------------|----------------|--------------|-----------|
| | | 5.15 | i5 Processor | T3,R2 | 1 |
| | | 5.16 | I7 Processor | T3,R2 | 1 |
| | | CLASS TEST | | | 1 |
| | | | | Total | 17 |
| | Content beyond Syllabus | | PIC Controller | T2,R1 | 1 |
| | | | | Total | 18 |
| CUMULATIVE PROPOSED PERIODS | | | | | 65 |

Text Books:


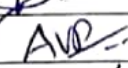
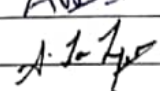
| S.No. | AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION |
|-------|---|
| 1 | Douglas V Hall, Microprocessors and Interfacing: Programming and Hardware, , 3 rd edition, TMH,2017. |
| 2 | Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D.Mckinlay, The 8051 Microcontrollers and Embedded Systems using Assembly and C , 2 nd edition, Pearson,2011. |
| 3 | Joseph Yiu's, The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors, 3 rd edition ,Elsevier,2014 |

Reference Books:

| S.No. | AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION |
|-------|---|
| 1 | A.K.Ray, K.M.Bhurchandi, "Advanced Microprocessors and Peripherals ", 3 rd Edition, TMH,2017 |
| 2 | Dr.Alexander G.Dean, Embedded System Fundamentals with ARM Cortex-M based Microcontrollers: A practical approach., ARM Education Media,2017 |

Web Details

| | |
|---|---|
| 1 | https://www.tutorialspoint.com/microprocessor/microcontrollers_overview.htm |
| 2 | https://circuitdigest.com/article/what-is-the-difference-between-microprocessor-and-microcontroller |

| | Name | Signature with Date |
|------|-----------------------|---|
| i. | Course Coordinator | Mr.B.Bhargav santosh  |
| ii. | Module Coordinator | Mr.A.V.D.Suresh  |
| iii. | Programme Coordinator | Mr.A.Satayanarayana  |


Principal