SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
Accredited by National Board of Accreditation, AICTE, New Delhi,Accredited by NAAC with "A" Grade – 3.32 CGPA,Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi,Permanent Affiliation to JNTUK, Kakinada
Seetharampuram, W.G.DT., Narsapur-534280, (Andhra Pradesh)

DEPARTMENT OFELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING PLAN

Course Code	CourseTitle	Semester	Branches	Contact Periods/Week	Academic Year	Date of commencement of Semester
20EC6T02	VLSI DESIGN	VI	ECE	6	2024-2025	18-11-2024

COURSE OUTCOMES

After completion of the course students can able to

1	Demonstrate VHDL synthesis, simulation, design tools, design verification tools. [K3]
2	Explain the fabrication process, layout design of logic circuits and Electrical properties of MOS Circuits [K2]
3	Illustrate the CMOS circuit design processes and scaling of MOS circuits [K4]
4	Summarize the use of different programmable logic devices.[K2]

UNIT	Out Comes / Bloom's Level	Topics No.	Topics/Activity	Text Book / Reference	Contact Hour	Delivery Method
I	CO 1: Demonstrate VHDL synthesis, simulation, design tools, design verification tools. [K3]		**UNIT-1: DIGITAL DESING USING HDL**			Chalk & Talk, PPT Tutorial, & Case Study
		1.1	Introduction to HDL and History of VHDL	T1, T2	1	
		1.2	VHDL requirements	T1,T2	1	
		1.3	VLSI Design flow and Circuit design process	T1,T2	1	
		1.4	Hardware simulation and Synthesis	T1, T2,R1	1	
		1.5	Levels of abstraction	T1, T2,R1	1	
		1.6	Various design styles of VHDL-data flow modeling, Behavioral modeling, structural modeling	T1, T2, R1,R2	1	
		1.7	VHDL Programs to design the circuits using all the three modeling –Half adder,Full adder	T1, T2,	1	
		1.8	Mux,Demux	T1, T2,	1	
		1.9	Decoder,Encoder	T1,T2, R1	1	
		1.10	Universal shift register	T1, T2, R1,R2	1	
		1.11	Counter	T1, T2,	1	
		1.12	Class Test-1		1	

				Total	12	
II	**CO2:** Explain the fabrication process, layout design of logic circuits and Electrical properties of MOS Circuits [K2]	**UNIT – 2:FABRICATION AND BASIC ELECTRICAL PROPERTIES OF MOSFET**				
		2.1	Introduction to IC Technology – MOS	T1,T3,R2	1	Chalk & Talk, PPT Tutorial, Active Learning & Case Study
		2.2	PMOS, NMOS	T1,T3,R2	2	
		2.3	CMOS & BiCMOS	T1,T2,R1,	2	
		2.4	ULSI Technology and its Applications	T1,T2,R1,	1	
		2.5	Basic Electrical Properties of MOS and BiCMOS Circuits- Ids-Vds relationships	T1,T2,R1,	1	
		2.6	MOS transistor threshold Voltage	, T2, R1,R2	1	
		2.7	Input Conductance, Output Conductance	T1,T3,R2	1	
		2.8	Figure of merit	T1,T3,R1,	1	
		2.9	Pass transistor,NMOS Inverter	T1,T3,R2,	1	
		2.10	CMOS Inverter analysis and design	T1,T3,R2,R3	1	
		2.11	Bi-CMOS Inverters	T1,T3,R2,R3	1	
		2.12	Class Test-2		1	
				Total	14	
III	**CO3:**Illustrate the CMOS circuit design processes and scaling of MOS circuits [K4]	**UNIT – 3:MOS CIRCUIT DESIGN PROCESS AND SCALING**				
		3.1	VLSI Design Flow	T1,T2.R1,	2	Chalk & Talk, PPT Tutorial
		3.2	MOS Layers	T1,T2.R1,	2	
		3.3	CMOS circuit diagram	T1,T2.R1,	2	
		3.4	Stick Diagram	T1,T2.R1,	2	
		3.5	Design Rules-Lambda Based, micron based and Layout diagram	T1, T3.R1,R2	2	
		3.6	2 micrometer CMOS Design rules for wires	T1, T3.R1,R2	2	
		3.8	Contacts and Transistors, Layout Diagrams of CMOS Inverters and Gates	T1, T3.R1,R2	2	
		3.9	SCALING: Scaling of MOS circuits, Limitations of Scaling	T1, T3.R1,R2	1	
		3.10	Class Test-3		1	
				Total	16	

IV	CO3:Illustrate the CMOS circuit design processes and scaling of MOS circuits [K4]	**UNIT – 4: BASIC CIRCUIT CONCEPTS AND CMOS TESTING**				
		4.1	Sheet Resistance, and its concept applied to MOS transistors and Inverters	T1, T3.R1,R2	1	Chalk & Talk, PPT Tutorial
		4.2	Area Capacitance of Layers, Standard unit of capacitance, and some examples with calculations.	T1, T2.R1,R2	1	
		4.3	The Delay Unit, Inverter Delays, Driving large capacitive loads, Propagation delays, Wiring capacitances and Choice of layers	T1, T3.R1,R2	2	
		4.4	CMOS TESTING : CMOS Testing, Need for testing	T1,T3.R1	1	Tutorial
		4.5	Test Principles, Design Strategies for test,	T1,T3.R1	1	
		4.6	Chip level Test Techniques.	T1,T3.R1	1	
		4.7	Class Test-4		1	
				Total	8	
V	CO4: Summarize the use of different semiconductor ICs (K2)	**UNIT – 5 : SEMICONDUCTOR IC DESIGN**				
		5.1	Introduction to Programmable Logic Devices (PLDs	T3.R1,R2	1	Chalk & Talk, PPT Tutorial, Active Learning & Case Study
		5.2	Programmable Logic Array (PLA)	T3,T3,R1	1	
		5.3	Programmable Array Logic (PAL)	T3,R1,R2	1	
		5.4	Implementation of logic functions using PLA/PAL	T3,R1,R2	1	
		5.5	Implementation approaches in ASIC Design	T3.R1,R2	1	
		5.6	Full custom design, semicustom design	T3.R1,R2	1	
		5.7	Gate arrays, Standard cells	T3,R1,R2	1	
		5.8	Complex Programmable Logic Devices (CPLDs)- architectures and applications	T3,R1,R2	1	
		5.9	Field programmable gate arrays (FPGAs) -architectures and applications	T3,R1,R2	1	
Content beyond Syllabus (if needed)		5.10	Introduction to System-on-Chip (SoC) and Network-on-Chip (NoC)-2D NoC, 3D NoC, Wireless NoC.	T3,R1,R2	1	
				Total	10	
				CUMULATIVE PROPOSED PERIODS	60	

Text Books:	
S.No.	**AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION**
1.	Kamran Eshraghian, Eshraghian Dougles, A.Pucknell, and Sholeh Eshraghian, Essentials of VLSI Circuits and Systems, 3rd Ed., Prentice Hall of India Publications , 2019.(Unit-1,2,3,4)
2.	J.Bhaskar, VHDL Primer, 3rd Ed., Prentice Hall of India Publications, 2017.(Unit-5)
3.	Dr.K.V.K.K.Prasad, Kattula Shyamala,VLSI Design – Black Book, 3rd Ed., Kogent Learning Solutions, 2015.
Reference Books:	
S.No.	**AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION**
1.	Debaprasad Das, VLSI Design, 2rd Ed., Oxford University Press, 2015.
2.	A.Albert Raj & T.Latha, VLSI Design, 3rd Ed., PHI Learning Private Limited, 2014.
3.	Richa Jain & Amrita Rai, Principles of VLSI & CMOS Integrated Circuits,1st Ed., S.Chand & companylimited, 2017.
Web Details	
1.	https://www.vlsisystemdesign.com › basic_courses
2.	https://www.udemy.com › topic › vlsi
3.	https://nptel.ac.in/courses/117101058/

		Name	Signature with Date
i.	Faculty I(for common Course)	Mr.K.V.B.Chandra Sekar Rao	
ii.	Faculty II (for common Course)	Ms. M.Radha Rani	
iii.	Faculty III (for common Course)	Mr. M.Murali	
iv.	Faculty IV (for common Course)	Mr.A.R.V.S.Gupta	
v.	Course Coordinator	Mr.K.V.B.Chandra Sekar Rao	
vi.	Module Coordinator	Dr.B.Ramana Kumar	
vii.	Programme Coordinator	Dr. B.S.Rao	

Principal