SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous)
SEETHARAMAPURAM, NARSAPUR-534280 W.G.DT. AP

DEPARTMENT OF BACHELOR OF COMPUTER APPLICATIONS(Honours)

TEACHING PLAN

Course Code	Course Title	Year/Sem	Branch	Contact hr/week	Academic Year
24BC1T04	DIGITAL LOGIC DESIGN	I/I	BCA(Honours)	5	2024-2025

Course Objectives:

The main objectives of the course are to

- Understand different methods used for the simplification of Boolean functions and binary arithmetic.
- Design and implement combinational circuits, synchronous & asynchronous sequential circuits.

Course Outcomes (Cos): At the end of the course, student will able to

CO No.	Course Outcome	Knowledge Level (K)#
CO1	Identify and recall the fundamentals of binary systems, number conversions, binary codes, and logic gates.	K1
CO2	Apply Boolean algebra theorems and simplification techniques to minimize Boolean functions using K-Maps and tabulation methods.	K3
CO3	Analyze and design combinational circuits like adders, subtractors, multiplexers, and comparators.	K4
CO4	Demonstrate the working of synchronous sequential circuits, including flip-flops, state reduction, and clocked circuits.	K3
CO5	Design and evaluate asynchronous sequential circuits and counters, including registers and latches.	K5

Week No	Outcome	Blooms Level	Topic / Activity		Text Books	Contact Hours	Delivery Method
			UNIT-I				
1,2	Identify and recall the fundamentals of binary systems, number conversions, binary codes, and logic gates.	K2	1.1	Introduction to Binary Number Syetem.	T1	1	Chalk & Board, PPT, Interactive Whiteboarding
			1.2	Representation of Binary number system	T1	1	
			1.3	Types of Number systems, Number Base Conversions	T1	4	
			1.4	Complements, Signed Binary Numbers	T1	2	
			1.5	Binary Codes, Binary Storage and Registers, Binary Logic.	T1	1	
			1.6	Introduction to Boolean Algebra, Basic Theorems and Properties of Boolean Algebra	T1	1	
			1.7	Boolean Functions, Canonical and Standard Forms	T1	1	
			1.8	Digital Logic Gates.	T1	1	
			UNIT-II				
3,4	Apply Boolean algebra theorems and simplification techniques to minimize Boolean functions using K-Maps and tabulation methods.	K3	2.1	Introduction to K-map method, Types of K-Map, Problems on K-map method	T1	3	Chalk & Board, PPT, Interactive Whiteboarding
			2.2	Tabular Method POS - SOP, Don't Care Conditions, NAND, NOR Implementation.	T1	3	
			2.3	Introduction to Combinational Circuit, Analysis and Design Procesure.	T1	1	

			2.4	Binary Adders, Subtractor	T1	2	
			2.5	Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers.	T1	3	
Mid I Exam							
UNIT-III							
5, 6	Analyze and design combinational circuits like adders, subtractors, multiplexers, and comparators.	K4	3.1	Synchronous Sequential Logic: Sequential Circuits - Latche	T1	2	Chalk & Board, PPT, Interactive Whiteboarding
			3.2	Flip-Flops, Types of flip flops	T1	4	
			3.3	An analysis of Clocked Sequential Circuits	T1	2	
			3.4	State Reduction	T1	2	
			3.5	State Assignment Design Procedure	T1	2	
UNIT-IV							
7,8	Demonstrate the working of synchronous sequential circuits, including flip-flops, state reduction, and clocked circuits.	K3	4.1	Registers and Counters: Registers	T1	2	Chalk & Board, PPT, Interactive Whiteboarding
			4.2	Shift Registers	T1	3	
			4.3	Ripple Counters	T1	2	
			4.4	Synchronous Counters	T1	2	
			4.5	Ring Counters-Johnson Counter.	T1	3	
UNIT-V							
9, 10	Design and evaluate asynchronous sequential circuits and counters,	K4	5.1	Asynchronous Sequential Circuit: Introduction	T1	1	Chalk & Board, PPT, Interactive Whiteboarding
			5.2	Analysis Procedure	T1	3	

	including registers and latches		5.3	Circuits with Latches	T1	4	
			5.4	Design Procedure.	T1	4	
Mid II Exam							
Total No. of Classes						**60**	

Recommended Text Books for Reading:

T1: M. Morris Mano, "Digital Design", 3rd edition, Pearson Education, Delhi, 2007

T2: Carl Hamacher, Z. Vranesic, S. Zaky: Computer Organization, 5/e (TMH).

Reference Text Books:

R1: Donald P Leech, Albert Paul Malvino and GoutamSaha,"Digital Principles and Applications", Tata McGraw Hill, 2007.

Faculty
(K. LAKSHMAN RAO)

Head of the Department

Principal