TEACHING PLAN

Course Code	Course Title	Semester	Branch	Contact Period /Week	Academic Year	Semester commencement date
20EC5E02	**Digital System Design (R20)**	**V**	**ECE**	**5**	**2024-25**	**03-06-2024**

COURSE OUTCOMES
After completion of the course student are able to

1	Develop the Combinational and Sequential logic circuit. (K3)
2	Evaluate the FSM and synchronous state machines.(K4)
3	Differentiate various logic families. (K4)
4	Construct the HDL Design flow.(K3)

Unit No	Out Come/ Bloom's Level		Topics/Actvity	Reference Text book	Contact Periods	Delivery Method
1	CO1: Develop the Combinational and Sequential logic circuit. (K3)		**COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUIT DESIGN**			Chalk & Talk, PPT, Active Learning & Tutorial
			Combinational circuits			
		1.1	Half adder	T1,R2,R5	1	
		1.2	Full adder	T1,R2,R5	1	
		1.3	BCD adder	T1,R2,R5	1	
		1.4	Code converters	T1,R2,R5	1	
		1.5	Magnitude comparator	T1,R2,R5	1	
		1.6	Multiplexers and decoders.	T1,R2,R5	1	
			Sequential circuits			
		1.7	Flip Flops-SR,	T1,R2,R5	1	
		1.8	JK Flip Flops	T1,R2,R5	1	
		1.9	T, D Flip Flops	T1,R2,R5	1	
		1.10	Master-slave FF	T1,R2,R5	1	
		1.11	Ripple counters	T1,R2,R5	1	
		1.12	Synchronous counters	T1,R2,R5	1	
		1.13	Shift registers	T1,R2,R5	1	
		TOTAL			**13**	

2.	CO2: Describe the FSM and synchronous state machines. (K1)	**FINITE STATE MACHINES**				Chalk & Talk, PPT, Active Learning & Tutorial
		2.1	Sequential circuit and examples - Finite State Model(FSM) and definitions	T1,R1,R3	1	
		2.2	Finite State Model(FSM) and definitions	T1,R1,R3	1	
		2.3	Capabilities and Limitations of Finite State machines	T1,R1,R3	1	
		2.4	Capabilities and Limitations of Finite State machines	T1,R1,R3	1	
		2.5	State Equivalence and Machine Minimization	T1,R1,R3	1	
		2.6	State Equivalence and Machine Minimization	T1,R1,R3	1	
		2.7	Input output transformations	T1,R1,R3	1	
		2.8	Mealy model	T1,R1,R3	1	
		2.9	Moore model	T1,R1,R3	1	
		2.10	Conversion from Mealy to Moore model and vice-versa	T1,R1,R3	1	
		2.11	Conversion from Mealy to Moore model and vice-versa	T1,R1,R3	1	
		TOTAL			**11**	

3.	CO2: Describe the FSM and synchronous state machines.(K1)	**SYNCHRONOUS STATE MACHINE DESIGN**				Chalk & Talk, PPT, Active Learning & Case study
		3.1	Concept of synchronous state machine-, General state machine architecture.	T1,R1,R4	1	
		3.2	Mathematical Representation of Synchronous sequential Machine	T1,R1,R4	1	
		3.3	Mathematical Representation of Synchronous sequential Machine	T1,R1,R4	1	
		3.4	Synthesis of Synchronous Sequential Circuit	T1,R1,R4	1	
		3.5	Synthesis of Synchronous Sequential Circuit	T1,R1,R4	1	
		3.6	Sequence detector	T1,R1,R4	2	
		3.7	Sequence detector	T1,R1,R4	1	
		3.8	State changes referred to number of state flip-flops			
		3.9	State changes referred to number of state flip-flops	T1,R1,R4	1	
		3.10	Redundant states	T1,R1,R4	1	
		3.11	Redundant states	T1,R1,R4	1	
		3.12	General state machine architecture.	T1,R1,R4	1	
		3.13	General state machine architecture.	T1,R1,R4	1	
				TOTAL	**13**	

4.	CO3: Classify various logic families. (K2)	**LOGIC FAMILIES**				Chalk & Talk,PPT, Active Learning & Project based learning
		4.1	Specifications,		1	
		4.2	Noise margin	T1,R2,R5	1	
		4.3	Noise margin	T1,R2,R5	1	
		4.4	Propagation delay	T1,R2,R5	1	
		4.5	Fan-in, fan-out	T1,R2,R5	1	
		4.6	Fan-in, fan-out	T1,R2,R5	1	
		4.7	Transistor-Transistor Logic (TTL)	T1,R2,R5	1	
		4.8	Emitter-Coupled Logic (ECL)	T1,R2,R5	1	
		4.9	CMOS Logic	T1,R2,R5	1	
		4.10	TTL	T1,R2,R5	1	
		4.11	CMOS Gates	T1,R2,R5	1	
		TOTAL			**11**	

5.	CO4: Construct the HDL Design flow.(K3)	**VLSI DESIGN FLOW**				Chalk & Talk, PPT, Active Learning & Tutorial
		5.1	Schematic, HDL	T2	1	
		5.2	Different modeling styles in Verilog	T2	1	
		5.3	Different modeling styles in Verilog	T2	1	
		5.4	Behavioral Modeling	T2	1	
		5.5	Structural Modeling	T2	1	
		5.6	Data types and objects	T2	1	
		5.7	Synthesis and Simulation	T2	1	
		5.8	Synthesis and Simulation	T2	1	
		5.9	Verilog constructs and codes for combinational	T2	1	
		5.10	Verilog constructs and codes for combinational	T2	1	
		5.11	Sequential circuits.	T2	1	
		5.12	Sequential circuits.	T2	1	
				TOTAL	**12**	
	Additional topics		Implementation of traffic light controller & elevator controller using Verilog			
TOTAL NO. OF CLASSES PROPOSED PER PERIOD'S					**60**	

Text Books:	
S.No.	**AUTHORS/BOOK TITLE/EDITION(latest)/PUBLISHER/YEAR OF PUBLICATION**
1	R. P. Jain, "Modern Digital Electronics" , Fourth Edition, Tata McGraw-Hill, 2010. **(UNIT I-IV)**
2	J Bhaskar, "A Verilog HDL Primer ", Third edition, Star Galaxy Publishing, 2018**.(Unit V)**
Reference Books:	
S.No.	**AUTHORS/BOOK TITLE/EDITION(latest)/PUBLISHER/YEAR OF PUBLICATION**
1	Zvi Kohavi & Niraj K. Jha , "Switching and Finite Automata Theory",ThirdEdition, Cambridge, 2010.
2	Morris Mano, Michael D Ciletti , "Digital Design", 4th Edition, PHI, 2012
3	Fredriac J. Hill, Gerald R. Peterson , "Introduction to Switching Theory and Logic Design",3rd Edition, January 2009.
4	Charles H.Roth, Larry L.Kinney, "Fundamentals of Logic Design", 7th Edition, Cengage Publisher, 2015.
5	A Anand Kumar, "Switching Theory and Logic Design", Third Edition, PHI, 2016
Web Details	
1	Digital Systems Design - https://nptel.ac.in/courses/108/106/108106177/
2	Digital Systems Design - https://ec.europa.eu/programmes/erasmus-plus/project-result-content/9f367412-e981-4a64-b01a-1157cbc933f5/Digital%20Systems%20Design.pdf
3	https://www.tutorialspoint.com/digital_circuits/index.htm

		Name	Signature with Date
i.	Faculty-i	V SATYA KISHORE	
ii.	Faculty-ii (for common course)	V SATYA KISHORE	
iii.	Course Coordinator	V SATYA KISHORE	
iv.	Module Coordinator	Dr. B. RAMANA KUMAR	
v	Programme Coordinator	Dr. B. S. Rao	

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